Device Modeling and System Simulation of Nanophotonic On-Chip Network for Reliability, Power, and Performance
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Abstract


Problems:
• Process and thermal variations in nanophotonics threaten the reliability of nanophotonic on-chip networks.
• Architecture community lacks the device and system-level models for nanophotonic devices and networks.

Solution:

Figure 1: Simulation framework that models reliability, power, and performance of nanophotonic on-chip networks.

Fabrication Efforts

Figure 2: We have fabricated hundreds of devices in ePIXfab and measured them in our labs.

Process and Thermal Variations in On-Chip Networks

Figure 3: Process & thermal variations lead to passband mismatch.

Process Variations

Complete mismatch which will block communication.

Thermal Variations

Figure 4: The impact of process variations on micro-ring transmission. 1 nm ring width variations leads to ~0.58 nm shift in resonant peak.

Figure 5: The impact of thermal variations on micro-ring transmission. We have a shift of 0.08 nm/C.

Device-level Models

We have used Transfer-matrix to model devices.
We have built a library for different devices we have designed and fabricated.

Figure 6: Micro-ring T-matrix model which matches measurements and has low computational overhead.

System-level Models

We leverage the device models to model the system in terms of reliability, power, and performance.

Figure 7: System-level models with variations. Bit-error rate, a measure of reliability, increases with variation then saturates. Latency, a performance metric, increases exponentially.

Simulation Framework

Figure 8: Simulation framework for reliability, power, and performance.

Simulation Results

Latency:

Broadcast-based architectures show worst performance with variations.

Networks with electro-optic conversion or with multiple paths between same nodes show more tolerance to variations.

Figure 9: Simulation results for performance. Performance with no variations (left) and with variations (right).

With variations, most of the benchmarks could not operate due to total passband mismatch.

Conclusion

• Nanophotonic is the future communication fabric for many-core architectures.
• We present a simulation framework that simulates on-chip network taking into account process and thermal variations for reliability, power, and performance.
• Our simulation framework reveals some important conclusions on different on-chip network designs.